Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently amended) A display control device, comprising:

a controller for providing a mode-control signal;

a scaling engine for producing a first interface signal;

a timing controller for converting said first interface signal into a second interface signal;

a selector for selecting either said first interface signal or said second interface signal to serve as a reference signal for output according to said mode-control signal; and

an interface circuit for converting said reference signal into an output signal according to said mode-control signal;

wherein, when said mode-control signal is under a first mode, said output signal is substantially said first interface signal; when said mode-control signal is under a second mode, said output signal is substantially said second interface signal; when said mode-control signal is under a third mode, said interface circuit converts said first interface signal to a third interface signal to serve as said output signal thereof; and when said mode-control signal is under a fourth mode, said interface circuit converts said second interface signal into a fourth interface signal to serve as said output signal.

2. (Original) The display control device as claimed in claim 1, further comprising a phase-locked loop for providing said interface circuit with a clock signal; wherein, when said mode-control signal is under either said first mode or said second mode, said clock signal has a first clock frequency; when said mode-control signal is under said third mode, said clock signal has a

second clock frequency; and when said mode-control signal is under said fourth mode, said clock signal has a third clock frequency.

3. (Original) A display control method, comprising the steps of:

a) providing a mode-control signal and a first interface signal;

b) converting said first interface signal into a second interface signal;

c) selecting either said first interface signal or said second interface signal as a reference signal according to said mode-control signal; and

d) converting said reference signal into an output signal according to said mode-control signal;

wherein, when said mode-control signal is under a first mode, said output signal is substantially said first interface signal; when said mode-control signal is under a second mode, said output signal is substantially said second interface signal; when said mode-control signal is under a third mode, said first interface signal is converted into a third interface signal to serve as said output signal; and when said mode-control signal is under a fourth mode, said second interface signal is converted into a fourth interface signal to serve as said output signal.

4. (Original) The display control method as claimed in claim 3, wherein step (c) further comprises the steps of:

generating a clock signal such that said reference signal is converted into said output signal in response to said clock signal; wherein, when said mode-signal is under either said first mode or said second mode, said clock signal has a first clock frequency; when said mode-control signal

is under said third mode, said clock signal has a second clock frequency; and when said mode-control signal is under said fourth mode, said clock signal has a third clock frequency.

5. (Canceled)

6. (Canceled)

7. (New) A display control device for processing an input image signal and providing an output image signal compatible with a panel module in a display system, comprising:

a mode controller for producing a mode signal associated with said panel module;

a scaling engine for converting an input image signal to a first interface signal;

a timing controller for converting said first interface signal into a second interface signal; and

a selector for selecting one of said first interface signal and said second interface signal in response to said mode signal.

8. (New) The display control device as claimed in claim 7, wherein said first interface signal is a transistor-transistor level (TTL) interface signal.

9. (New) The display control device as claimed in claim 7, wherein said second interface signal is a TTL/TCON interface signal.

10. (New) The display control device as claimed in claim 7, further comprising an interface circuit for either bypassing said selected interface signal to serve as said output image signal or converting said selected interface signal into a differential interface signal to serve as said output image signal in response to said mode signal.

11. (New) The display control device as claimed in claim 10, further comprising a phase-locked loop for providing a clock signal to said interface circuit; wherein said clock signal has a first frequency when said selected interface signal is bypassed to serve as said output image signal and has a second frequency when said differential interface signal is provided to serve as said output image signal, wherein said second frequency is greater than said first frequency.

12. (New) The display control device as claimed in claim 11, wherein said differential interface signal is a low-voltage differential signaling (LVDS) interface signal when said selected interface signal is a TTL interface signal.

13. (New) The display control device as claimed in claim 12, wherein said second frequency is substantially seven times of said first frequency.

14. (New) The display control device as claimed in claim 11, wherein said differential interface signal is a reduced swing differential signaling (RSDS) interface signal when said selected interface signal is a TTL/TCON interface signal.

15. (New) The display control device a claimed in claim 14, wherein said second frequency is substantially two times of said first frequency.

16. (New) A display control device for processing an input image signal and providing an output image signal compatible with a panel module in a display system, comprising:

a mode controller for producing a mode signal associated with said panel module;

a scaling engine for converting an input image signal to a first interface signal; and

an interface circuit for either bypassing said first interface signal to serve as said output image signal or converting said first interface signal into a second interface signal to serve as said output image signal in response to said mode signal.

17. (New) The display control device as claimed in claim 16, wherein further comprising a phase-locked loop for providing a clock signal to said interface circuit; wherein said clock signal has a first frequency when said first interface signal is bypassed to serve as said output image signal and has a second frequency when said second interface signal is provided to serve as said output image signal, wherein said second frequency is greater than said first frequency.

18. (New) The display control device as claimed in claim 17, wherein said second interface signal is a low-voltage differential signaling (LVDS) interface signal when said first interface signal is a TTL interface signal.

19. (New) The display control device as claimed in claim 17, wherein said differential interface signal is a reduced swing differential signaling (RSDS) interface signal when said selected interface signal is a TTL/TCON interface signal.

20. (New) A method for processing an input image signal and providing an output image signal compatible with a panel module in a display system, comprising the following steps of:

producing a mode signal associated with said panel module;

converting an input image signal to a first interface signal;

converting said first interface signal into a second interface signal; and

selecting one of said first interface signal and said second interface signal in response to said mode signal.

21. (New) The method as claimed in claim 20, wherein said first interface signal is a transistor-transistor level (TTL) interface signal.

22. (New) The method as claimed in claim 20, wherein said second interface signal is a TTL/TCON interface signal.

23. (New) The method as claimed in claim 20, further comprising a step of bypassing said selected interface signal to serve as said output image signal or converting said selected interface signal into a differential interface signal to serve as said output image signal in response to said mode signal.

24. (New) The method as claimed in claim 23, further comprising a step for providing a clock signal; wherein said clock signal has a first frequency when said selected interface signal is bypassed to serve as said output image signal and has a second frequency when said differential interface signal is provided to serve as said output image signal, wherein said second frequency is greater than said first frequency.

25. (New) The method as claimed in claim 24, wherein said differential interface signal is a low-voltage differential signaling (LVDS) interface signal when said selected interface signal is a TTL interface signal.

26. (New) The method as claimed in claim 25, wherein said second frequency is substantially seven times of said first frequency.

27. (New) The method as claimed in claim 24, wherein said differential interface signal is a reduced swing differential signaling (RSDS) interface signal when said selected interface signal is a TTL/TCON interface signal.

28. (New) The method a claimed in claim 27, wherein said second frequency is substantially two times of said first frequency.

29. (New) A method for processing an input image signal and providing an output image signal compatible with a panel module in a display system, comprising the following steps of:

producing a mode signal associated with said panel module;

converting an input image signal to a first interface signal; and

either bypassing said first interface signal to serve as said output image signal or converting said first interface signal into a second interface signal to serve as said output image signal in response to said mode signal.

30. (New) The method as claimed in claim 29, wherein further comprising a step for providing a clock signal; wherein said clock signal has a first frequency when said first interface signal is bypassed to serve as said output image signal and has a second frequency when said second interface signal is provided to serve as said output image signal, wherein said second frequency is greater than said first frequency.

31. (New) The method as claimed in claim 30, wherein said second interface signal is a low-voltage differential signaling (LVDS) interface signal when said first interface signal is a TTL interface signal.

32. (New) The method as claimed in claim 30, wherein said differential interface signal is a reduced swing differential signaling (RSDS) interface signal when said selected interface signal is a TTL/TCON interface signal.